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|                                                         |
|               NanoSim Version V-2004.06                 |
|                  SN: P20040520-Linux                    |
|         Machine Name: micro10.ilab.columbia.edu         |
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|                                                         |
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 Built by nsmgr in " 20040520_linux_ns_main " on Thu May 20 20:54:12 PDT 2004
 Mon Dec 14 17:53:58 2009

 Command line options:  -nspice ./design.spi -nvec ./stimulusmicropr~ -C ./power.cfg -o ./power


 The 32-bit version of the simulator is running.


 Initializing system messages took 0.000 s

 Installing interactive/configuration commands ...
 Installing commands took 0.020 s


 Netlist compilation will be case insensitive.
 All letters will be converted to lower case.
 Start netlist compilation at Mon Dec 14 17:53:58 2009

 Compiling "design.spi" (SPICE)
 Compiling "/usr/tech/tsmc025/tsmc025/mix025_1.l" (SPICE)
 Compiling "/usr/tech/tsmc025/tsmc025/mix025_1.l" (SPICE)
 Compiling "/usr/tech/tsmc025/tsmc025/mix025_1.l" (SPICE)
 Compiling "/usr/tech/tsmc025/tsmc025/mix025_1.l" (SPICE)
 Compiling "/usr/tech/tsmc025/tsmc025/mix025_1.l" (SPICE)
 Compiling "/usr/tech/tsmc025/tsmc025/mix025_1.l" (SPICE)
 Compiling "stimulusmicropr~" (VECTOR)



 Parsing netlist finished in 0 seconds

 Circuit temperature from netlist                  :       25.000

 Building instance tree finished in 0 seconds

 Finish netlist compilation at Mon Dec 14 17:53:58 2009

 Netlist compilation took 0.070 s
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 NOTICE:Techfile Voltage (*nanosim tech="voltage") set to  2.5V ...

 This simulation uses Hspice models

 Building node/element arrays took 0.480 s

 Reading configuration files ...
 ;This is a GUI generated file.
 ;It is overwritten and updated for each run.


 report_node_powr vdd!

 print_node_v *
 Reading configuration files took -0.000000 s



 WARNING:NanoSim:0x2110925a:There are 6 DANGLING nodes. Please view the file ./power.dng for the node names

 # of CMOS elements                                      :         1699
 # of dc voltage sources                                 :            1
 # of stimulus elements                                  :            1
 # of elements                                           :         1701
 # of used elements                                      :         1700
 # of nodes                                              :          723
 # of subckt                                             :           40
 # of top-level instances                                :           11


 Circuit partitioning ...

 Among 281 stages, there are:
          281 pwl stages
            0 grouped pwl stages
            0 analog stages
            0 NR stages
            0 grouped analog stages
            0 rc stages
            0 ud stages
            0 ADFMI functional model stages
           56 nodes in the largest pwl stage
            0 nodes in the largest digital stage

          272 stages (272 pwl/analog stages) with 0-9 nodes
            8 stages (8 pwl/analog stages) with 10-19 nodes
            1 stages (1 pwl/analog stages) with 50-99 nodes
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 Among 723 nodes, there are:
          723 pwl nodes
            0 analog (accurate) nodes
            0 rc nodes
            0 ud nodes

            0 cut nodes
            0 mem_cut nodes
            0 no_clamp nodes
          710 nodes in stages
            7 voltage source nodes
            2 constant nodes
            0 NR nodes

 Among 1701 elements, there are:
         1699 elements in stages
         1699 pwl elements
            0 synchronous elements
            0 SMS elements
            0 analog (accurate) elements
            0 rc elements
            0 ud elements
            0 ADFMI functional model elements
            0 VERILOGA model elements
            0 behavioral model elements

            0 mna elements
            0 NR elements
            0 mos transistors identified as keepers
          869 mos transistors need Subthreshold current
            0 keepers removed
            0 keepers reduced


 Circuit partitioning took -0.000 s
 Constructing matrix ...
 Matrix ordering and construction took 0.010 s


 After reading configuration file(s), 726 signals are identified to be printed:
          723 voltage signals
            3 node current signals, including:
                  1 node inst. current signals
                  1 node RMS current signals
                  1 node AVG current signals

 Statistics of memory used for signal printing:
       361208 bytes allocated in total, including:
                48008 bytes allocated for node current/voltage/logic signals
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               124 bytes allocated additionally for current printing
            164008 bytes allocated additionally for node current signals
            149068 bytes allocated additionally for element branch current signals

 Levelizing stages ...
 Levelizing stages took -0.000 s
 DC initialization ...
 WARNING:NanoSim:0x2110e4b1:There are 6 DANGLING nodes which have been set to 0.0 volt by the simulator before DC initialization.
 Please view the file ./power.dcu for the node names.

 Finishing initialization (level 0 -- 9)
 1 dynamic stages assigned in DC Initialization

 Number of residual dc events scheduled          : 0
 Number of ic nodes scheduled                    : 6
 DC initialization took -0.000 s

 Simulation begins in pwl mode ...
 Simulation ends at 4000.000 ns

 Simulation took 0.050 s

 Current information calculated over the intervals:

      0.00000e+00 -  4.00001e+03 ns

 Node: vdd!
     Average current     : -2.92651e+03 uA
     RMS current         :  2.98727e+03 uA

     Current peak #1     : -2.22710e+04 uA  at   6.00000e+02 ns
     Current peak #2     : -1.96480e+04 uA  at   1.80000e+03 ns
     Current peak #3     : -1.45940e+04 uA  at   1.20000e+03 ns
     Current peak #4     : -5.46200e+03 uA  at   1.20121e+03 ns
     Current peak #5     : -4.77600e+03 uA  at   1.60075e+03 ns


 Simulation time resolution                      : 1.000e-02 ns
 Print time resolution                           : 1.000e-02 ns
 Number of PWL matrix solutions                  : 4963
 Number of PWL MOS model lookups                 : 31829
 Number of time steps                            : 4963
 Number of iterations                            : 0
 Number of rejected time steps                   : 1

 Global simulation parameters used:

 SPD            0.25V     ASPD            0.1V
 SIM_DESV       0.25V     SIM_AESV      0.125V
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```
 VDS_MIN  0.00022689V     AVDS_MIN      1e-08V
 SSC (steady state current)         0.1uA
 SUBI (subthreshold current)          1uA
 DC CURRENT                           1uA

               1.0 real        0.6 user        0.0 sys


 No errors reported in the .err file (./power.err)
```