

IntSim Algorithm

1. Initial Input all parameters

2. Logic gate sizing

Margin: Fraction of clock cycle lost due to skew and process variations
For computing size W

$$(12) t_d = \frac{1-\text{margin}}{f} = L_d 0.7 \frac{R_{NAND}}{W} (f.o. C_{NAND} W + f.o. \chi k_l (7.3 + W)^{1-p})$$

$$(8) i(l) = \begin{cases} \frac{\alpha k}{2} \Gamma \left(\frac{l^2}{3} - 2l^2 \sqrt{N_{sockets}} + 2l N_{sockets} \right) l^{2p-4} & 1 \leq l < \sqrt{N_{sockets}} \\ \frac{\alpha k}{6} \Gamma (2\sqrt{N_{sockets}} - l)^3 l^{2p-4} & \sqrt{N_{sockets}} \leq l < 2\sqrt{N_{sockets}} \end{cases}$$

3. Generation of stochastic wiring distribution

where

$$\Gamma = \frac{2N_{gates}(1 - N_{gates}^{p-1})}{\left(-N_{sockets}^p \frac{1 + 2p - 2^{2p-1}}{p(p-1)(2p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{N_{sockets}}}{2p-1} - \frac{N_{sockets}}{p-1} \right)}$$

4. Set baseline parameters for iterations
Initial Power 100w, repeater # 0

Available area Required area

$$(14) 2e_w A = \chi P_{local} \sqrt{\frac{A}{N_{sockets}}} \int_{l_{min}}^{l_{max}} l i(l) dl$$

5. Local interconnect modeling

$$(15) e_w = 1 - e_{router} - e_{power/gnd} - e_{vias}$$

$$(16) e_{vias} = \sqrt{\frac{(2N_{wires_higher} + 2N_{repeater}) \cdot (P_{local} + s\lambda)^2}{A}}$$

l_{max} in eq.14
= l_{min} in eq.17

6. Arrangement of wires without repeaters

$$(17) 2e_w A = \chi P \sqrt{\frac{A}{N_{sockets}}} \int_{l_{min}}^{l_{max}} l i(l) dl$$

$$(18a) \tau_{rc} = 4.4 \frac{\rho(P, AR)}{ar \cdot p^2} c l_{max}^2 \sqrt{\frac{A}{N_{sockets}}} = \frac{\beta}{f}$$

7. Global interconnect modeling

$$(13) P = \text{Max} \left[2 \cdot (k_p + 0.5) \cdot N_{power_pads} \cdot \rho \cdot \frac{l_r \cdot d_{pad_to_pad}^2}{\pi e_{router} \cdot AR \cdot k_p \cdot V_{IR}} \cdot \ln \left(\frac{0.65 \cdot d_{pad_to_pad}}{l_{pad}} \right), \frac{D}{2} \sqrt{\frac{c_{clock} \rho}{AR \cdot k_c R_o C_o}} \cdot \frac{1}{f R_o C_o} \left(\sqrt{72.6 + \frac{4.4 \beta_o}{f R_o C_o}} + 11 \right) \right]$$

Step 8 repeater #
For Step 5

8. Assignment of wires with repeates

$$(17) 2e_w A = \chi P \sqrt{\frac{A}{N_{sockets}}} \int_{l_{min}}^{l_{max}} l i(l) dl$$

$$(18b) \tau_{rc} = \frac{2l_{max} \sqrt{\rho(P, ar) c R_o C_o}}{ar \cdot P} \left(\frac{0.7}{\delta} + 0.7\gamma + \frac{0.4}{\gamma} + 0.7\delta \right) \sqrt{\frac{A}{N_{sockets}}} = \frac{\beta}{f}$$

l_{min}

9. Power computation and iteration

$$\text{Estimated power} = \frac{\text{Old estimated power} + \text{Calculated power}}{2}$$

Step 2 device widths
For Logic gate power

10. Data output
Wire levels #, wire level pitches, power

IntSim Algorithm

1. Initial Input all parameters

2. Logic gate sizing

Margin: Fraction of clock cycle lost due to skew and process variations For computing size W

$$(12) t_d = \frac{1 - \text{margin}}{f} = L_d 0.7 \frac{R_{NAND}}{W} (f.o. C_{NAND} W + f.o. \chi k_1 (7.3 + W)^{1-p})$$

3. Generation of stochastic wiring distribution

$$(8) i(l) = \begin{cases} \frac{\alpha k}{2} \Gamma \left(\frac{l^3}{3} - 2l^2 \sqrt{N_{sockets}} + 2l N_{sockets} \right) l^{2p-4} & 1 \leq l < \sqrt{N_{sockets}} \\ \frac{\alpha k}{6} \Gamma (2\sqrt{N_{sockets}} - l)^3 l^{2p-4} & \sqrt{N_{sockets}} \leq l < 2\sqrt{N_{sockets}} \end{cases}$$

where

$$\Gamma = \frac{2N_{gates}(1 - N_{gates}^{p-1})}{\left(-N_{sockets}^p \frac{1 + 2p - 2^{2p-1}}{p(p-1)(2p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{N_{sockets}}}{2p-1} - \frac{N_{sockets}}{p-1} \right)}$$

4. Set baseline parameters for iterations Initial Power 100w, repeater #: 0

Available area Required area

$$(14) 2e_w A = \chi P_{local} \sqrt{\frac{A}{N_{sockets}}} \int_l^{l_{max}} l i(l) dl$$

$$(15) e_w = 1 - e_{router} - e_{power/gnd} - e_{vias}$$

$$(16) e_{vias} = \sqrt{\frac{(2N_{wires_higher} + 2N_{repeater}) \cdot (P_{local} + s\lambda)^2}{A}}$$

lmax in eq.14 = lmin in eq.17

5. Local interconnect modeling

6. Arrangement of wires without repeaters

$$(17) 2e_w A = \chi P \sqrt{\frac{A}{N_{sockets}}} \int_{l_{min}}^{l_{max}} l i(l) dl$$

$$(18a) \tau_{rc} = 4.4 \frac{\rho(P, AR)}{ar \cdot P^2} c l_{max}^2 \sqrt{\frac{A}{N_{sockets}}} = \frac{\beta}{f}$$

7. Global interconnect modeling

$$(13) P = \text{Max} \left[2 \cdot (k_p + 0.5) \cdot N_{power_pads} \cdot \rho \cdot \frac{l_r \cdot d_{pad_to_pad}^2}{\pi e_{router} \cdot AR \cdot k_p \cdot V_{IR}} \cdot \ln \left(\frac{0.65 \cdot d_{pad_to_pad}}{l_{pad}} \right), \frac{D}{2} \sqrt{\frac{c_{clock} \rho}{AR \cdot k_c \cdot R_o \cdot C_o}} \cdot \frac{1}{f R_o C_o} \left(\sqrt{72.6 + \frac{4.4 \beta_o}{f R_o C_o}} + 11 \right) \right]$$

Step 8 repeater # For Step 5

8. Assignment of wires with repeats

$$(17) 2e_w A = \chi P \sqrt{\frac{A}{N_{sockets}}} \int_{l_{min}}^{l_{max}} l i(l) dl$$

$$(18b) \tau_{rc} = \frac{2l_{max} \sqrt{\rho(P, ar) c R_o C_o}}{ar \cdot P} \left(\frac{0.7}{\delta} + 0.7\gamma + \frac{0.4}{\gamma} + 0.7\delta \right) \sqrt{\frac{A}{N_{sockets}}} = \frac{\beta}{f}$$

lmin

9. Power computation and iteration

$$\text{Estimated power} = \frac{\text{Old estimated power} + \text{Calculated power}}{2}$$

Step 2 device widths For Logic gate power

10. Data output Wire levels #, wire level pitches, power

